A 71-Gb/s NRZ Modulated 850-nm VCSEL-Based Optical Link

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***Abstract*— We report error free (BER < 10^{-12}) operation of a directly non-return-to-zero modulated 850-nm vertical cavity surface-emitting laser (VCSEL) link operating to 71 Gb/s. This is the highest error free modulation rate for a directly modulated laser of any type. The optical link consists of a 130-nm BiCMOS driver IC with two-tap feed-forward equalization, a wide bandwidth 850-nm VCSEL, a surface illuminated GaAs PIN photodiode, and a 130-nm BiCMOS receiver IC.**

***Index Terms*— High-speed modulation, optical interconnects, semiconductor lasers, vertical cavity surface-emitting laser.**

I. Introduction

SERIAL data rates continue to increase for the major data communications standards: Ethernet, Infiniband, Fibre Channel and PCI Express. While still under discussion, the Infiniband HDR serial rate could be 51.5625 Gb/s. Today, direct Non-Return-to-Zero (NRZ) modulation of 850 nm VCSELs and multimode fiber make up the vast majority of the volume of data communication links in the field. It is worthwhile exploring the limits of this technology. For directly modulated edge emitting DFB lasers, the highest reported data rate is 56.1 Gb/s [1], and for directly NRZ modulated VCSELs it is 64 Gb/s [2]. In this letter we report error free (BER < 10^{-12}), direct NRZ modulation of an 850 nm VCSEL-based link up to 71 Gb/s. This is the highest reported error free direct modulation rate for any laser to date.

II. Optical Link Components

The optical link consists of a transmitter subassembly (driver IC and VCSEL) connected to a receiver subassembly (receiver IC and photodiode) through 7 m of standard OM3 50/125 μm multimode fiber. The following subsections describe each of the sub-components in detail.

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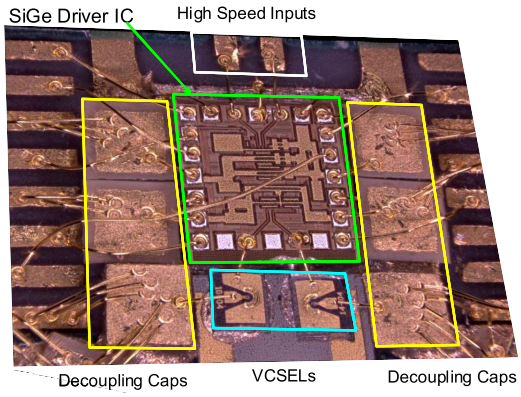

Fig. 1. Photograph of transmitter showing driver IC, VCSELs, decoupling capacitors and printed circuit board traces.

A. Transmitter Subassembly

Fig. 1 shows a picture of the center of the transmitter subassembly on a printed circuit board (PCB). In the center is the driver IC which is surrounded on two sides by power supply decoupling capacitors. The decoupling capacitors used are 560 pF (0202 size) although high speed operation is not particularly sensitive to this value. The other two sides are for the high speed signal input and the connection to the VCSELs. The 1 mm^2 driver IC is implemented in 130 nm BiCMOS and incorporates 2-tap linear Feed Forward Equalization (FFE) in the differential output stage. It is similar to the one described in [4] but with a shorter delay in the FFE path. All connections to the driver chip are through short (~300–500 μm) wirebonds. The high speed connections to PCB are through surface mounted vertical SMP connectors located 4.7 mm away from the driver chip through single-ended 50 Ω transmission lines on the top surface. The impedance of the driver IC differential input is 100 Ω. Careful design went into the PCB footprint for the SMP connectors to minimize the discontinuity. Between the SMP connectors and the driver IC are 100 nF (0201 size) dc blocking capacitors. The VCSELs are mounted as close as possible to the driver IC in a common anode configuration. This configuration allows for separate optimization of the VCSEL and circuit supplies and lowers the power dissipation. Because the VCSEL is cathode driven, it is very important to make the anode power supply as close to an ideal ac ground as possible. To this extent, two capacitors are triple wirebonded in parallel to the PCB, a 1200 pF (0202 size) and a 10 nF (0202 size). Only single wirebonds are used for

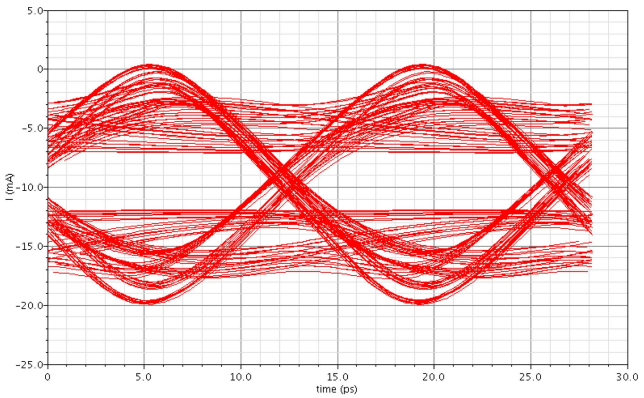

Fig. 2. Simulation of driver IC output current at 71 Gb/s showing the feed forward equalization characteristics.

connections to the VCSEL due to the small pad sizes. Also important for cathode driving is to minimize the VCSEL parasitic capacitance to ground which goes contrary to customary anode driving. To reduce this parasitic capacitance, the VCSELs are mounted on an AlN submount which has half its thickness removed beneath the VCSELs to create an air gap between the VCSELs and the PCB.

For this very high speed operation, most of the driver chip supply voltages were set for 4 V. The total power consumption of the transmitter was 950 mW (13.4pJ/bit) including the VCSEL which is biased at 8.2 mA. Fig. 2 shows a simulation of the output current of the driver IC at 71 Gb/s. Substantial over- and under-shoot can be seen in the driving waveform which originates from the FFE characteristics.

B. VCSEL

The VCSEL used in the experiments is the same as was used for the 64 Gb/s measurements in [2]. In the VCSEL structure (provided by IQE Europe), five strained InGaAs quantum wells are contained within a short 0.5-λ cavity for high differential gain at 850 nm. Lateral optical and current confinement is provided by two 5 μm diameter primary oxide apertures, while four larger diameter secondary oxide apertures are used to reduce the parasitic capacitance. The thickness of the topmost GaAs layer was tuned to optimize the photon lifetime for a large modulation bandwidth and a flat modulation response. At 8.2 mA, the output power is 5.0 mW and the 3 dB modulation bandwidth is ~26 GHz. The D- and K-factors [3] for the VCSEL are 11.5 GHz/mA$^{1/2}$ and 0.14 ns respectively. Fig. 3 shows the L-I-V curves and an optical spectrum for this VCSEL.

C. Receiver Subassembly and Photodiode

Fig. 4 shows a photograph of the receiver subassembly with the receiver IC located in the center. The PCB layout is the same as for the transmitter. The receiver IC design, described in [4], is similar to the transmitter but contains a transimpedance amplifier with a 480 Ω feedback resistor at the input stage. A GaAs PIN photodiode (PD) is placed as close as possible to the receiver IC to shorten the wirebond length. The photodiode is mounted on an Alumina submount to reduce its capacitance to ground and to elevate it slightly

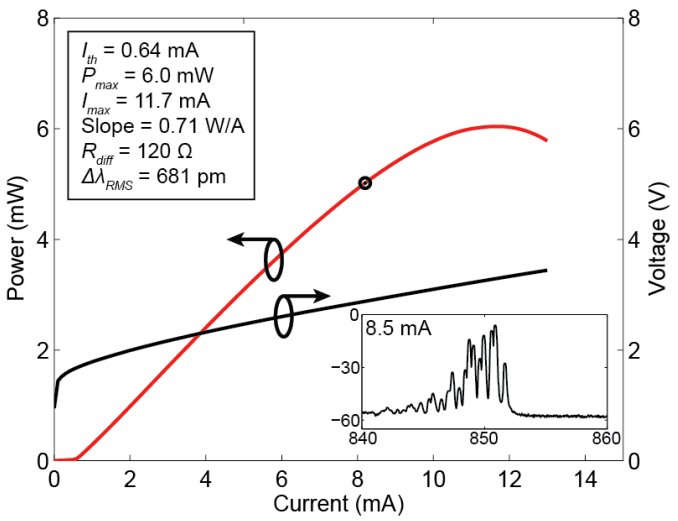

Fig. 3. Room temperature L-I-V characteristics of the VCSEL. Dot shows bias point for 71 Gb/s operation Inset: optical spectrum at 8.5 mA.

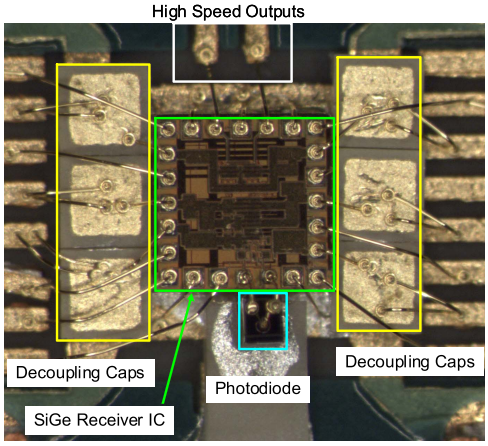

Fig. 4. Photograph of receiver showing receiver IC, photodiode, decoupling capacitors and printed circuit board traces.

above the IC for wirebonding purposes. The photodiode is dc biased through the IC using a pair of 2 kΩ resistors, one at each terminal. The high speed signal is ac coupled on chip to the the TIA input. This receiver is identical to the one used for the 64 Gb/s measurements in [2] but with two important changes: the photodiode diameter was reduced from 21 μm to 12 μm and the photodiode intrinsic layer thickness was reduced from 1.6 μm to 1.0 μm. Accompanying these changes was a drop in bias voltage from 7.0 to 5.7 V. The properties of the two photodiodes have been reported in detail in [5]. The change to a smaller area, thinner photodiode lowered the capacitance slightly from 73 to 61 fF, reduced the responsivity slightly from 0.55 to 0.48 A/W and increased the bandwidth from 22 to >30 GHz. The increase in bandwidth was the enabling factor to move from 64 to 71 Gb/s. Most of the receiver supply voltages are 4 V and the power consumption is 860 mW with a single ended output amplitude of 200 mV. In experiments with the 21 μm photodiode, a lensed 50 μm fiber probe can be used with very high coupling efficiency. For coupling to the 12 μm photodiode, an aspheric lens with an 11 mm focal length (Thorlabs F220FC-B) was used to collimate the light and another aspheric lens with a 2.8 mm

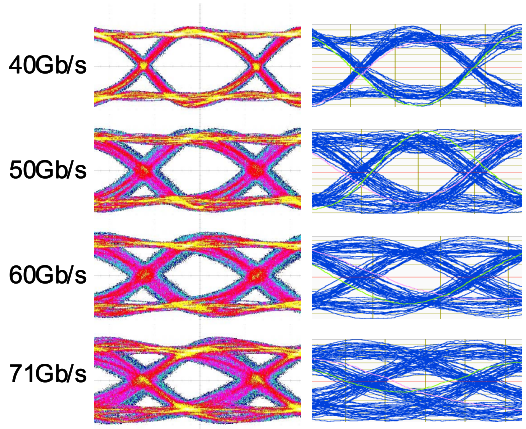

Fig. 5. Eye diagrams from 40-71 Gb/s. Received electrical eyes (left) and transmit optical eyes (right). The horizontal scale is 1.8 unit intervals. The vertical scale is 100mV/div for the electrical eyes. Full scale is ~1.5mV for the optical eyes.

focal length (Newport 5721-H-B) was used to focus the light light with an estimated couipling efficiency of 88%.

III. Results

The high speed data is generated by an SHF 12103A pattern generator with the output set to the minimum value of 400 mV. The pattern used is PRBS7. A pair of 10 cm coax cables connect the pattern generator to the transmitter PCB. The transmitter is held at 28 °C. The receiver is connected through 30 cm coax cables to an SHF 11104A error detector. At these very high data rates with low extinction ratios, it is crucial to protect the VCSEL from optical feedback which increases the relative intensity noise. To this extent, the VCSEL light is coupled to the fiber using a diffractive lens (similar to the one described in [6]). The transmitter and receiver IC settings from the previous 64 Gb/s condition were used as a starting point and adjusted to obtain error free operation as the data rate was increased up to 71 Gb/s. Compared with the 64 Gb/s settings, the main changes to the transmitter were an increase in the bias of the main output stage and a slight decrease in VCSEL bias current from 8.5 to 8.2 mA (42 kA/cm^2). The FFE coefficient for the transmitter is 0.44. The main changes to the receiver setting were an increase in bias to the output stage and an increase in the strength of the FFE tap coefficient from 0.35 to 0.47. Once error free operation was established at 71 Gb/s, these settings were held constant and used for all the measurements reported here. Fig. 5 shows a set of transmit optical and received electrical eyes at data rates from 40 to 71 Gb/s. The horizontal scale is 1.8 unit intervals. The received electrical eyes are collected with a Tektronix DSA8300 oscilloscope using an 80E09 sampling head at a bandwidth setting of 60 GHz and an 82A04-60G precision timebase. The transmit optical eyes were collected using a Picometrix PX-D7 60 GHz photodiode. Due to the low responsivity of this photodiode (<0.05 A/W), the optical waveform was averaged 256 times and then folded to generate an eye diagram. The transmit extinction ratio, measured at 20 Gb/s a data rate low enough to avoid any eye closure due to ISI, is 1.6. As the data rate is increased, the optical eye accumulates more intersymbol interference (ISI) while the electrical eye accumulates

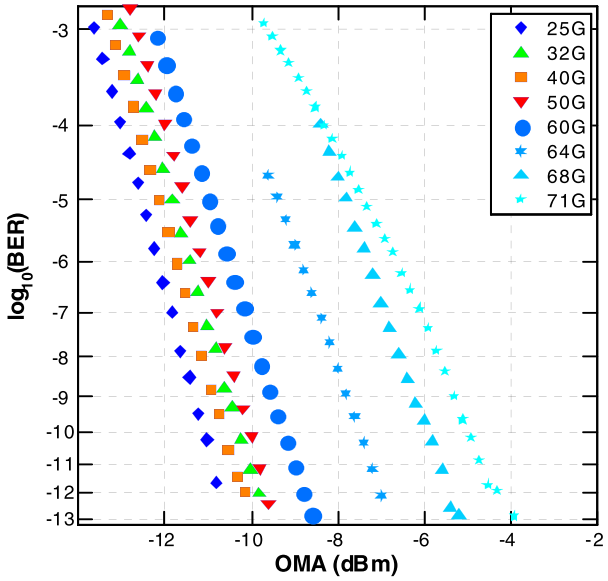

Fig. 6. BER vs. OMA for data rates of 25 Gb/s to 71 Gb/s using the 12 μm PD.

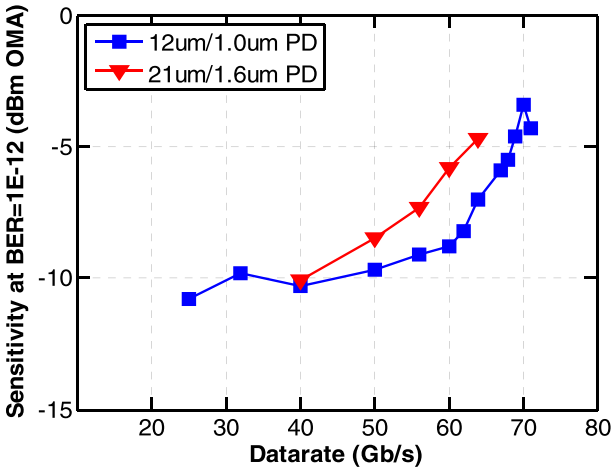

Fig. 7. Receiver sensitivity as a function of data rate for two different photodiodes. Red = 21 μm diameter photodiode with 1.6 μm intrinsic region, Blue = 12 μm diameter photodiode with 1.0 μm intrinsic region.

more jitter. There is 4.8 dB of ISI at 71 Gb/s. Fig. 6 is a plot of BER vs. Optical Modulation Amplitude (OMA) for eight data rates between 25 and 71 Gb/s. There is no evidence of a BER floor down to the level of 10^{-12}. The points on the BER curves are 0.2 dB apart and each measurement is terminated when there are two successive points with zero errors in 100 s. At the termination points for 25 and 71 Gb/s there is 8.2 and 0.8 dB on the optical attenuator, respectively. As the data rate is increased from 25 Gb/s, the receiver sensitivity starts to decrease slowly up to about 60 Gb/s then decreases rapidly. This characteristic is plotted in Fig. 7 for both the receiver with the 12 μm photodiode and the one with the 21 μm photodiode. The sharp decrease in sensitivity coincides in both cases with the bandwidth of the receiver front end which is dominated by the photodiode's bandwidth.

Fig. 8 shows the measured bathtub curves at 50, 60, and 71 Gb/s collected at a photocurrent of 560 μA. The measured data points span from BER = 10^{-3} to ~10^{-10}. The solid curves are fits to the data using a dual-Dirac function [7] and

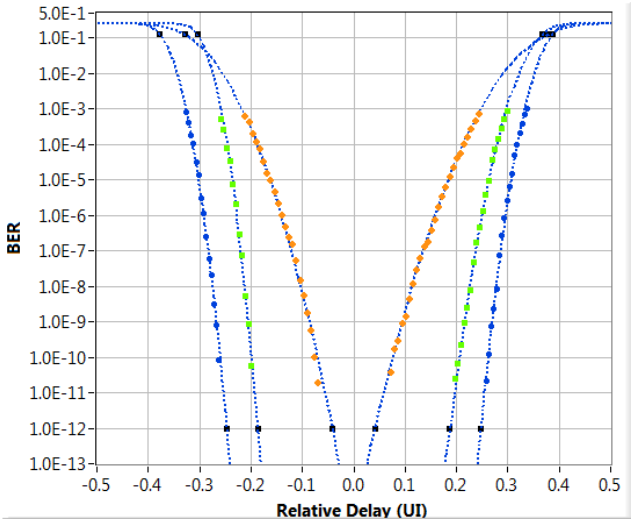

Fig. 8. Bathtub curves for 50, 60 and 71 Gb/s (outer to inner).

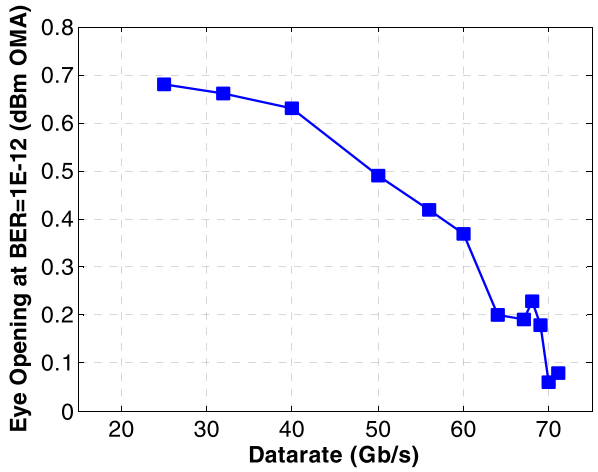

Fig. 9. Eye opening at BER $= 10^{-12}$ as a function of data rate from 25 to 71 Gb/s.

the points at BER $= 10^{-12}$ are from the fit. At 50 Gb/s the eye opening (EO) at BER $= 10^{-12}$ is 0.49 UI, the deterministic jitter (DJ) is 4.7 ps and the random jitter (RJ) is 5.4 ps. At 71 Gb/s there is almost no timing margin with EO $= 0.08$ UI, DJ $= 4.2$ ps and RJ $= 8.7$ ps. The extracted DJ at 71 Gb/s is lower than that at 50 Gb/s and lower than the 6.9 ps observed in the optical eye. This can be partially explained by the dual-Dirac fit to the data but mostly due to the settings of the receiver FFE which were tuned to give the best eye opening at 71 Gb/s. The large increase in RJ is partially attributed to the error detector as the optical eyes do not exhibit this much increase in jitter.

The evolution of the EO with data rate is plotted in Fig. 9 for 25 to 71 Gb/s and exhibits an almost parabolic shape. At 25 Gb/s, the EO is as large as 0.68 UI. Continuing the trend downward, the EO appears to go to zero around 73 Gb/s, a data rate beyond where the error detector currently operates.

IV. Discussion and Conclusion

We have reported on the details and characteristics of a multimode fiber link that is able to operate error free up to 71 Gb/s using an 850 nm VCSEL as the light source and a surface illuminated GaAs PIN photodiode as the detector. This is the highest reported error free modulation speed for a directly modulated NRZ optical link to date. As serial speeds continue to increase it is worthwhile to see if 100 Gb/s NRZ modulation could be attainable. From a circuits point of view, 100 Gb/s NRZ signaling has already been demonstrated in multiple technologies for more than 10 years now [8]. Progress in high speed VCSELs has been rather rapid with at least three separate institutions reaching the 50 Gb/s level in just the past two years [9]–[11]. Part of this progress can be attributed to high speed test equipment that is now available commercially while another part can be traced to commercial interest in high speed lasers. To reach 100 Gb/s, both the VCSEL and photodiode would need about a 30-40% increase in bandwidth to the ~40 GHz level. Photodiodes have been shown to achieve these bandwidth albeit with a reduction in responsivity. The VCSEL in this experiment has a K-factor of 0.14 ns which implies an intrinsic damping-limited laser bandwidth of more than 60 GHz but the real limitation is the parasitic bandwidth and thermal saturation. There is also a trade-off between modulation bandwidth and the laser damping which has to be taken into account [12]. Given the rapid progress and the prospects for reducing parasitics, providing better heat sinking, and the use of equalization techniques, a 100 Gb/s NRZ modulated link seems viable.

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